

**Memorandum of Understanding  
between  
the Thomas Jefferson National Accelerator Facility  
and  
Indiana University**

**R & D for the Hall D Project  
Electronics and Time-of-Flight**

**I. Introduction**

This Memorandum of Understanding (MOU) outlines the activities that the members of the Indiana University High Energy Physics Group (Task D) are carrying out in collaboration with the Thomas Jefferson Accelerator Facility (JLab) for R & D associated with the Hall D Project.

The Hall D Collaboration presented its plan for a detector facility to be used in the search for gluonic excitations in photoproduction reactions in a Letter of Intent submitted to the JLab PAC in January, 1999. The PAC recommended that JLab appoint a committee to review the physics and proposed technique. That committee, chaired by David Cassel of Cornell, met in December 6-7, 1999 with the collaboration and concluded that the physics is “high priority” and the Hall D project provides a “unique opportunity” for “making definitive searches for exotic states in this mass region.” The committee deemed “the general design of the detector is technically sound” and went on to recommend R&D efforts to address concerns about optimization and/or technology choices for various detector subsystems.

This MOU with Indiana University is to partially fund R&D associated with the readout and trigger electronics and the time-of-flight (TOF) system.

**II. Personnel**

1. The contact person for the Indiana U group is Alex Dzierba.

2. The following personnel are included in the Indiana Hall D group:

Person	Positions	Percent of Research Effort
Chris Bass	Graduate Student	100%
Alex Dzierba	Professor	100 %
Richard Heinz	Professor	25 %
Eric Scott	Technician	100 %
Paul Smith	Electronics Engineer	100 %
Craig Steffen	Graduate Student	25 %
Thom Sulanke	Software Engineer	30 %
Scott Teige	Scientist	75 %

The percentages refer to the approximate percentage of research time to be spent by the person on Hall D activities during FY2000-FY2001.

### III. Project Description

#### 1. Electronics R&D for the Hall D Project - Overview

In order to minimize costs associated with cabling and in order to handle eventual photon fluxes of  $10^8$  photons/sec Hall D will use on-board FADCs and TDCs and employ a digital pipeline architecture.

#### 2. Review Committee's Comments:

- The basic concept for the Level-1 trigger is sound. This includes input from flash converters, a fully-pipelined formation of trigger primitives from several subsystems, appropriate front-end buffering during Level-1 latency, feature extraction from a settable time window, and local event buffering, zero-suppression, and packet formation in response to issuance of a global Level-1.
- The choice of pipeline architecture is not clearly motivated. Within a pipelined architecture, the choice of 250 MHz for TDCs to preserve drift chamber spatial resolution is clear, but it remains to be shown if this is the optimum choice, both in terms of cost and performance, for other systems. Similarly, choices of ADC and TDC step size and bit count should be optimized.
- There is some reliance on continued commercial development of high-speed FADCs, memories, and gate-array logic, but this does not seem to be an area for present concern.

- The speeds proposed will require that fully functional prototypes be developed soon to insure proper performance at speed, handling of pipeline synchronization, and noise immunity of front-end sections.
- Core manpower is identified for this subsystem.

### 3. Electronics

The Hall D calorimeters, drift chamber pads,  $dE/dx$ , Cerenkov, and possibly other detectors will be read out by Flash Analog to Digital Converters which will record both time and amplitude information. The number of bits and sampling rate required is being investigated with simulations; 8 bits at 250 MHz are believed to be adequate for the drift chambers. The barrel calorimeter, photon tagger, start counter and TOF system will require better time resolution than provided by FADCs alone but must also maintain the feature of *deadtimeless* operation. The digital information will be *pipelined* in dual port memories while a digital trigger is formed.

Indiana University will have primary engineering responsibility for the FADC and trigger systems and is collaborating with JLab on the construction and testing of the TDC system. Prototypes of the FADCs and TDCs are required to investigate issues of noise, power, packaging, and reliability. The trigger prototype will use the FADCs, dual-port memories, and a pipelined digital energy sum trigger.

The pipeline architecture is needed to handle the high beam rates with minimal deadtime. No beam or interaction signal is available since the beam is electrically neutral - all trigger decisions must be derived from the detector. Pipelining makes the time depth of the pipeline memory available for forming the level 1 trigger. The architecture is similar to that used in other recent experiments including Zeus and BaBar ([1] - [5]). The systems requiring high-precision TDC must also operate without deadtime. Currently no commercial TDC meets the requirements of Hall D. The commercially available F1 TDC integrated circuit, properly buffered with dual port memory and packaged in VME standard modules shows promise in meeting the needs of the experiment.

The optimization of time step and bit count is currently being studied through simulation and measurements of fast PMTs. Tradeoffs between engineering costs for optimized front end electronics for each subsystem and costs for using standardized front end electronics on multiple subsystems must also be considered.

High speed Flash ADCs are the subject of considerable commercial development. The main application of these devices is in digital radiofrequency RF communication and radar systems; the RF is digitized and all signal processing and demodulation is handled by digital processors. Since the December 1999 review of the Hall D project flash ADCs with greater than 1 GHz sample rates have come on the market.

Dual Port memory integrated circuits are used commercially in network routers; again semiconductor companies are constantly placing faster versions of these devices on the market. Gate arrays capable of operating at speeds of 250 MHz or higher have been released since the Hall D review; many of these gate arrays now include dual port memory.

The general philosophy of the Hall D electronics design is to use commercially available components and to avoid custom integrated circuits which require large investments in engineering.

During the period of this effort an 8 channel prototype FADC packaged on a standard VME card will be built. 96 channels of TDC will also be built on one or two VMEP cards, depending on the achievable packaging density.

#### 4. References

- [1] Dow, S. F. *et al*, IEEE Transactions on Nuclear Science Vol **46 No. 4** (1999) 785.
- [2] Albert, J. *et al*, SLAC-PUB-7996 (1998).
- [3] Angstadt, R. G. *et al*, IEEE Transactions on Nuclear Science Vol **39 No. 5** (1992) 1297.
- [4] Morgado, C. J. S. *et al*, IEEE Transactions on Nuclear Science Vol **41 No. 4** (1994) 1250.
- [5] Lankford, A. J., Nuclear Instruments and Methods **A409** (1998) 654.

#### 5. Time of Flight (TOF) Plans

The Indiana and IHEP (Serpukhov) groups have a plan for testing several TOF modules using high quality PMTs and Russian PMTs. The issue is a potential savings of up to \$1000/channel for 320 channels. These tests will be carried out in the HEP labs in Bloomington using radioactive sources and cosmic rays and in a beam in Fall, 2000 at Serpukhov.

Inexpensive PMTs are available from Russian sources, however, it has not been established that these tubes are suitable for TOF applications. Evaluation of the response characteristics of several candidate PMTs, including some Russian tubes, is currently underway at Indiana. Quantitative measurements of rise time, pulse shape and voltage dependence are being made, but, there is no substitute for an full scale prototype test.

Beam time is available at Serpukhov in fall, 2000. It is proposed that two full length TOF hodoscope elements will be built and tested in this beam. These elements will be approximately 2 meters in length and will represent the worst case for time resolution since shorter

modules suffer less signal degradation due to attenuation. Two configurations are envisaged, one to allow direct comparison of different PMT types, another to allow measurement of the achievable time resolution for the proposed system, both objectives identified during the Hall D review.

#### **IV. Responsibilities and Funding**

##### *1. Responsibilities of Indiana University*

Indiana University will develop a prototype Flash ADC VME module by December, 2000. Two modules will be built, one to remain at Indiana for further tests and the other to be delivered to JLab for further tests as well.

Indiana University will also do tests of scintillator and PMT's to optimize the TOF systems. These tests will take place in Bloomington in the HEP labs using radioactive sources and cosmic rays. Other tests will take place in a beam at Serpukhov, Russia in Fall, 2000. A report will be issued by January, 2001 summarizing the results of these tests.

##### *2. Funding and Other Considerations - Indiana University*

Indiana University will provide funds associated with support of personnel and travel to carry out the tasks outlined in this MOU.

Indiana University has requested R&D funding from the Department of Energy to carry out electronics R&D and TOF R&D beyond the scope covered by this MOU.

The laboratory space needed to carry out the work covered by this MOU exists and is assigned to the HEP groups involved in Hall D.

##### *3. Funding and Other Considerations - JLab*

JLab will provide funds needed to purchase equipment as outlined in the tables below. Note that the VME crate and single board computer would be used to test the prototype FADC. The VME ADC & FADC are commercial modules and would provide a "benchmark" to compare the prototype FADC to. The other items are components which would be used to construct the prototype FADC.

*Funds required for equipment for electronics R&D*

Item	Number	Unit Cost	Total
VME crate	1	\$3,000	\$3,000
VME single board computer	1	\$2,500	\$2,500
VME ADC module	1	\$2,500	\$2,500
VME FADC module	1	\$2,500	\$2,500
FADC integrated circuits	10	\$250	\$2,500
High speed programmable gate arrays	15	\$250	\$3,750
Printed circuits	1	\$5,000	\$5,000
<b>Total</b>			<b>\$21,750</b>

*Funds required for equipment for TOF R&D*

Item	Number	Unit Cost	Total
Scintillator	1	\$5,000	\$5,000
Phototubes	10	\$1,200	\$12,000
Phototube bases	10	\$300	\$3,000
<b>Total</b>			<b>\$20,000</b>

*4. Special Considerations*

A. JLab will have the final responsibility for the acceptance of all deliverables and retains the right, in conjunction with the Hall D collaboration management to terminate or renegotiate this MOU if the requirements of specification, schedule and costs cannot be met by the Indiana group.

B. All items bought or fabricated using JLab funds will remain the property of JLab.

C. The continuation of the agreement is dependent on the approval of funds for all parties.

D. The agreement may be amended as necessary.

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